WHAT IS CLAIMED IS:

1. A synchronous semiconductor memory device operating in synchronization with a clock signal, comprising:

a memory cell array having a plurality of memory cells arranged;

an output control circuit burst-reading a plurality of read data from said memory cell array, and sequentially generating a plurality of read instructions indicating levels of said plurality of read data respectively, in synchronization with said clock signal;

a data output circuit outputting data in response to each of the sequentially generated said plurality of read instructions;

a transmission control unit provided between said output control circuit and said data output circuit and transmitting each of said plurality of read instructions generated by said output control circuit to said data output circuit; and

a signal propagation control circuit determining whether each of said plurality of read instructions sequentially generated by said output control circuit corresponds to a first one or a second or following one of said plurality of read data; wherein

said transmission control unit transmits, in accordance with a result of determination by said signal propagation control circuit, said read instruction corresponding to said first one of said plurality of read data with a first transmission time to said data output circuit, and transmits said read instruction corresponding to said second or following one of said plurality of read data with a second transmission time being different from said first transmission time to said data output circuit.

2. The synchronous semiconductor memory device according to claim 1, wherein

said first transmission time is longer than said second transmission time.

3. The synchronous semiconductor memory device according to

claim 1, further comprising

a voltage setting circuit precharging each of first and second nodes electrically connected to said data output circuit to a prescribed voltage before said burst-reading, and separating each of said first and second nodes from said prescribed voltage after a start of said burst-reading; wherein

each of said plurality of read instructions includes a first control signal and a second control signal set to complementary levels dependent on the level of the corresponding read data;

said transmission control unit transmits said first control signal and said second control signal generated by said output control circuit to said first node and said second node, respectively, with one of said first transmission time and said second transmission time, dependent on said result of determination by said signal propagation control circuit; and

said signal propagation control circuit includes a determining unit determining, based on voltage levels of said first node and said second node, whether said first control signal and said second control signal generated by said output control circuit correspond to said first one or said second or following one of said plurality of read data.

4. The synchronous semiconductor memory device according to claim 3, wherein

said determining unit has

a logic circuit outputting a determination signal in accordance with a result of logical operation between the voltage level of said first node and the voltage level of said second node, and

a transmission circuit transmitting said determination signal from said logic circuit to said transmission control unit, during a period of time starting from generation of said first control signal and said second control signal by said output control circuit up to a next generation of said first control signal and said second control signal; and wherein

said transmission control unit switches said first transmission time and said second transmission time in accordance with said determination

signal from said transmission circuit.

5. The synchronous semiconductor memory device according to claim 1, wherein

said transmission control unit has

a delay circuit for providing a delay time corresponding to difference between said first transmission time and said second transmission time, and

a path switch transmitting said read instruction corresponding to said first one of said plurality of read data to said data output circuit through said delay circuit and transmitting said read instruction corresponding to said second or following one of said plurality of read data to said data output circuit bypassing said delay circuit, dependent on said result of determination by said signal propagation control circuit; and wherein

said delay time of said delay circuit is adjustable in a non-volatile manner by an input from outside of said delay circuit.

6. The synchronous semiconductor memory device according to claim 5, wherein

said delay circuit has at least one propagation time adjusting circuit formed of a plurality of CMOS inverters each having a prescribed drivability and connected in parallel with each other,

said plurality of CMOS inverters connected in parallel each being disconnected in accordance with said input.